- - REMARKS - -

The present amendment replies to a First Non-Final Office Action dated March 20, 2002. Claims 1-13 as originally filed are currently pending in the present application. However, claims 1-13 have been cancelled herein without disclaimer or prejudice. Claims 14-26 have been added herein to more clearly distinguish the present invention over the cited art.

In the First Non-Final Office Action, Examiner Ellis objected to the specification for containing a title that is not descriptive of the present invention. In response to this objection, the Applicant has amended the title of the specification from "VARIABLE-INSTRUCTION-LENGTH- PROCESSING" to "METHOD FOR FORMING VARIABLE LENGTH INSTRUCTIONS IN A PROCESSING SYSTEM", and have corrected any typographical errors in the specification. Attached hereto is a marked-up version of an amendment to the specification that is captioned "**Version With Markings To Show Changes Made**". No new matter has been introduced by amendment of the specification.

In the First Non-Final Office Action, Examiner Ellis further rejected pending claims 1-13 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,745,722 to *Matsumoto* et al. The Applicant has thoroughly considered Examiner Ellis' remarks concerning the patentability of independent claims 1-13 over *Matsumoto*. The Applicant has also thoroughly read *Matsumoto*.

The Applicant respectfully traverses the 35 U.S.C. §102(b) rejection of claims 1-13, because *Matsumoto* fails, among other things, to disclose, teach or suggest an expansion bit of the present invention. To more clearly distinguish the present invention over *Matsumoto*, the Applicant has cancelled claims 1-13 without disclaimer or prejudice for consideration in a continuation application, and has added independent claim 14 with claims 15-19 depending therefrom. The Applicant asserts that claims 14-19 are patentable over *Matsumoto*, because *Matsumoto* fails to disclose, teach or suggest "providing a first parameter byte including a first set of data value bits, and a first

expansion bit indicative of whether the processing system expands the first set of data value bits or reads any additional parameter bytes including additional sets of data value bits" as recited in independent claim 14. In fact, *Matsumoto* teaches away from the underlined novelty of independent claim 14 by exclusively teaching a data decoder 3 that immediately passes unexpanded (i.e., not decoded) data value bits to an execution unit 5 without reading any additional data value bits. See, *Matsumoto* at column 4, lines 56-65.

The Applicant has also added independent claims 20 and 21 with claims 22-26 depending therefrom. The Applicant asserts that claims 20-26 are patentable over *Matsumoto*, because *Matsumoto* fails to disclose, teach or suggest "providing a parameter portion including a plurality of data value bits, and a first indicator representative of a number of the plurality of data value bits" as recited in independent claim 20, and "providing a parameter portion including a plurality of data value bits, and a first indicator representative a number of bytes in the parameter portion" as recited in independent claim 21. The underlined novelty of independent claims 20 and 21 are supported by Examiner Ellis' recognition in the First Non-Final Office Action that *Matsumoto* does not disclose, teach or suggest the underlined novelty of independent claims 20 and 21.

Therefore, the Applicant respectfully requests withdrawal of the rejection of claims 1-13 under 35 U.S.C. §102(b) as being unpatentable over *Matsumoto*, and an allowance of claims 14-26 as being patentable over *Matsumoto*.

SUMMARY

Examiner Ellis' objection to the title of the specification has been obviated by the amendment of the specification. Examiner Ellis' 35 U.S.C. §102(b) rejection of claims 1-13 has been obviated by the cancellation of claims 1-13 and the addition of claims 14-26. The Applicant respectfully submits that claims 14-26 as added herein fully satisfy the requirements of 35 U.S.C. §§ 102, 103 and 112. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested.

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Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

On page 1, line 1: "[VARIABLE-INSTRUCTION-LENGTH- PROCESSING] METHOD FOR FORMING VARIABLE LENGTH INSTRUCTIONS IN A PROCESSING SYSTEM"

Paragraph beginning on page 6, lines 19-21 has been amended as follows:

"Figures 2A and 2B show exemplary formats for parameters of each of the respective types [Um_C, Sm_C] UmNC, SmNC. In these examples, each of the parameters comprises two bytes. Specifically:"

Paragraph beginning on page 8, line 23 to page 9, line 14 has been amended as follows:

"Preferably the opcode portion of the instruction is formatted to inherently specify the number of parameters and their characteristics. For example, an opcode for an ADD instruction, where the ALU 16 adds an operand A to an operand B and where the sum is stored in an address C, would include three parameters - one for each of the operands A[,] and B, and address C. Note that, for example, A and B may have values that are compressible and C may be an index from a base address, which is potentially a compressible number. Further, the definition of the instruction itself will specify the pertinent characteristics of each of these parameters. As another example, an opcode for an ENTER instruction, where the processor 10 is to decrement the stack pointer value SP in register 124 to an address in the stack that will provide memory space represented by a

value M, would include the single unsigned parameter M. The size of M may be compressed, as this is an index to the current address located by SP. The definition of the instruction itself will also specify the other pertinent characteristics of the parameter M."